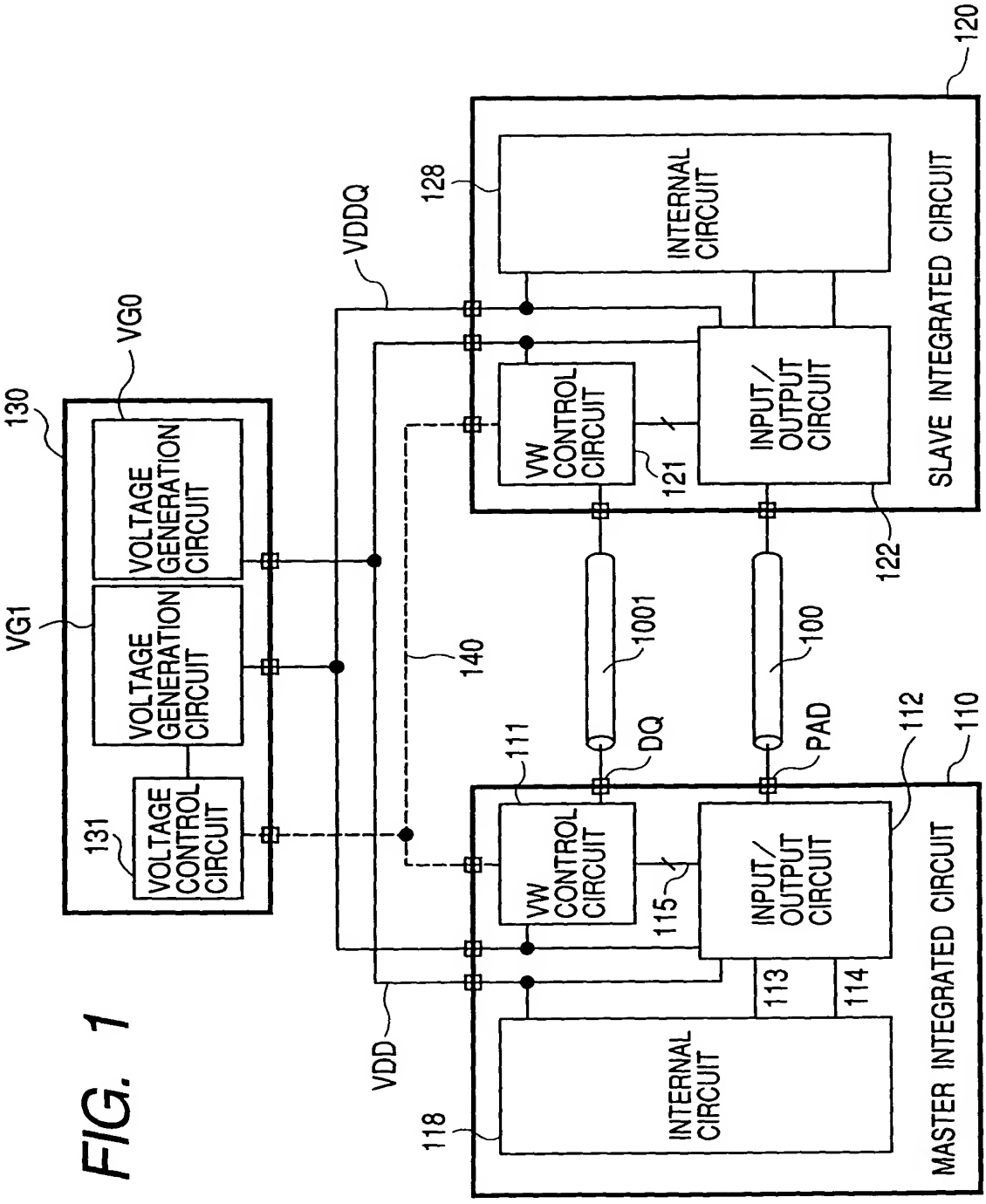

120
SLAVE INTEGRATED CIRCUIT
128
INTERNAL CIRCUIT
VDDQ
VG0
130
VG1
VOLTAGE GENERATION CIRCUIT
VOLTAGE GENERATION CIRCUIT
VOLTAGE CONTROL CIRCUIT
131
VW CONTROL CIRCUIT
121
INPUT/ OUTPUT CIRCUIT
122
140
1001
100
DQ
PAD
111
112
110
VW CONTROL CIRCUIT
115
INPUT/ OUTPUT CIRCUIT
113
114
VDD
INTERNAL CIRCUIT
118
MASTER INTEGRATED CIRCUIT

FIG. 1

FIG. 2

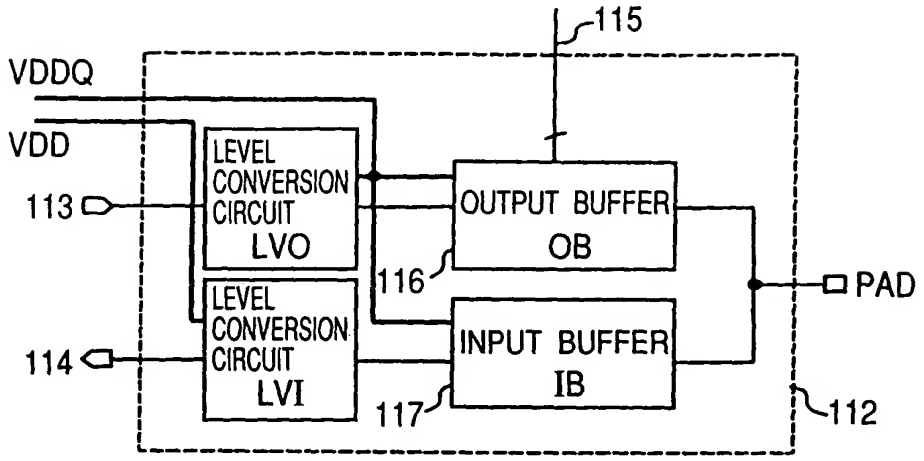

115
VDDQ
VDD
113
LEVEL CONVERSION CIRCUIT LVO
OUTPUT BUFFER OB
116
PAD
LEVEL CONVERSION CIRCUIT LVI
114
INPUT BUFFER IB
117
112

FIG. 3

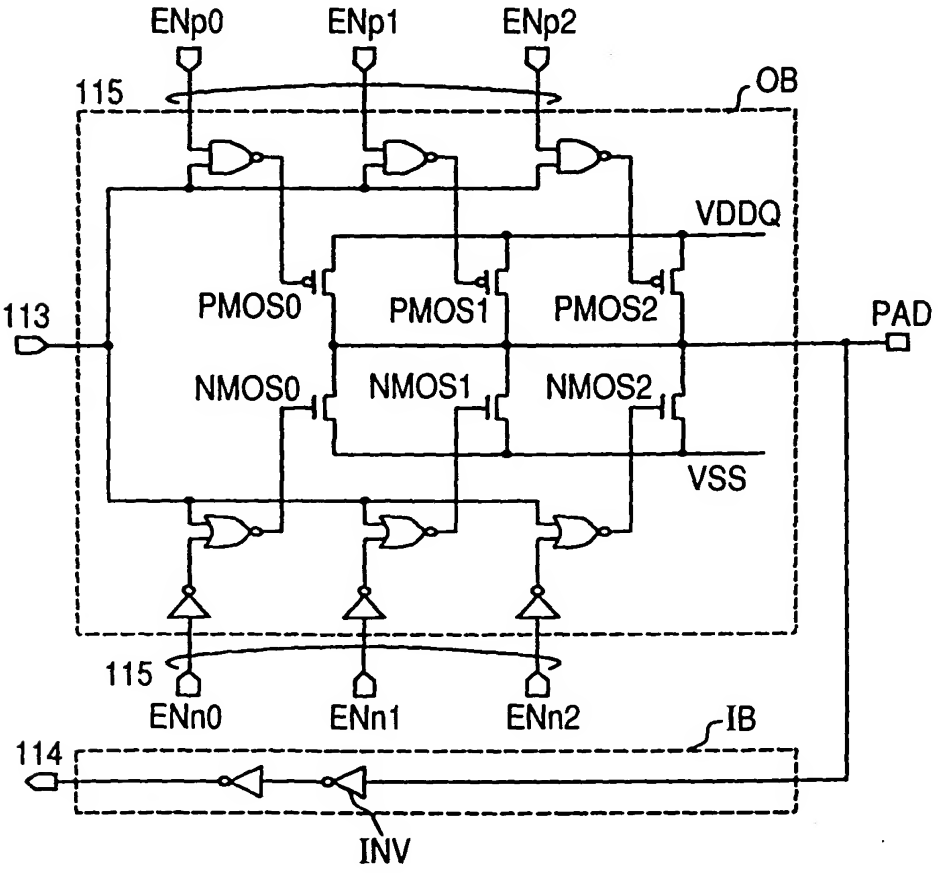

ENp0
ENp1
ENp2
115
OB
VDDQ
113
PMOS0
PMOS1
PMOS2
PAD
NMOS0
NMOS1
NMOS2
VSS
115
ENn0
ENn1
ENn2
IB
114
INV

FIG. 4

(A) 〔MASTER INTEGRATED CIRCUIT〕

ENi code	NMOS size (um)	I/O Power supply voltage VDDQ (V)			
		1.5	1.8	2.2	2.5
(001)	44	566	345	231	189
(010)	88	283	173	116	95
(011)	132	189	115	77	63
(100)	176	142	86	58	47
(101)	220	113	69	46	38
(110)	264	94	58	39	32
(111)	308	81	49	33	27

A1 B1

(B) 〔SLAVE INTEGRATED CIRCUIT〕

ENi code	NMOS size (um)	I/O Power supply voltage VDDQ (V)			
		1.5	1.8	2.2	2.5
(001)	40	228	182	151	136
(010)	80	114	91	76	68
(011)	120	76	61	50	45
(100)	160	57	46	38	34
(101)	200	46	36	30	27
(110)	240	38	30	25	23
(111)	280	33	26	22	19

A2 B2

FIG. 5

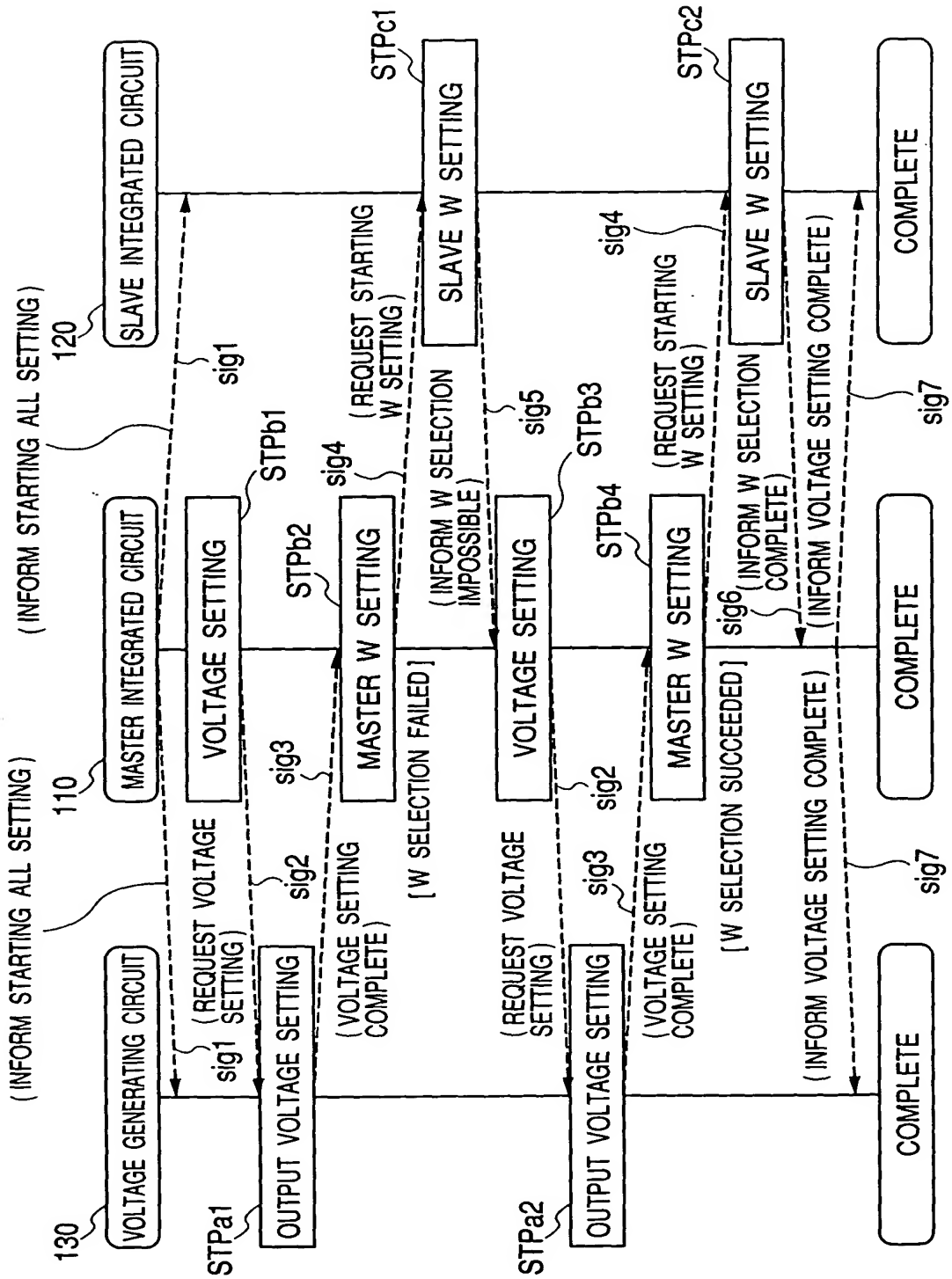

(INFORM STARTING ALL SETTING)
130
VOLTAGE GENERATING CIRCUIT
110
MASTER INTEGRATED CIRCUIT
120
SLAVE INTEGRATED CIRCUIT
(INFORM STARTING ALL SETTING)
(REQUEST VOLTAGE SETTING)
sig1
OUTPUT VOLTAGE SETTING
STPa1
VOLTAGE SETTING
STPb1
sig1
(VOLTAGE SETTING COMPLETE)
sig2
MASTER W SETTING
STPb2
sig3
[W SELECTION FAILED]
(INFORM W SELECTION IMPOSSIBLE)
sig4
(REQUEST STARTING W SETTING)
SLAVE W SETTING
STPc1
(REQUEST VOLTAGE SETTING)
sig5
OUTPUT VOLTAGE SETTING
STPa2
VOLTAGE SETTING
STPb3
sig2
(VOLTAGE SETTING COMPLETE)
sig3
MASTER W SETTING
STPb4
[W SELECTION SUCCEEDED]
(INFORM W SELECTION COMPLETE)
sig6
(REQUEST STARTING W SETTING)
sig4
SLAVE W SETTING
STPc2
(INFORM VOLTAGE SETTING COMPLETE)
sig7
COMPLETE
COMPLETE
sig7
COMPLETE

FIG. 6

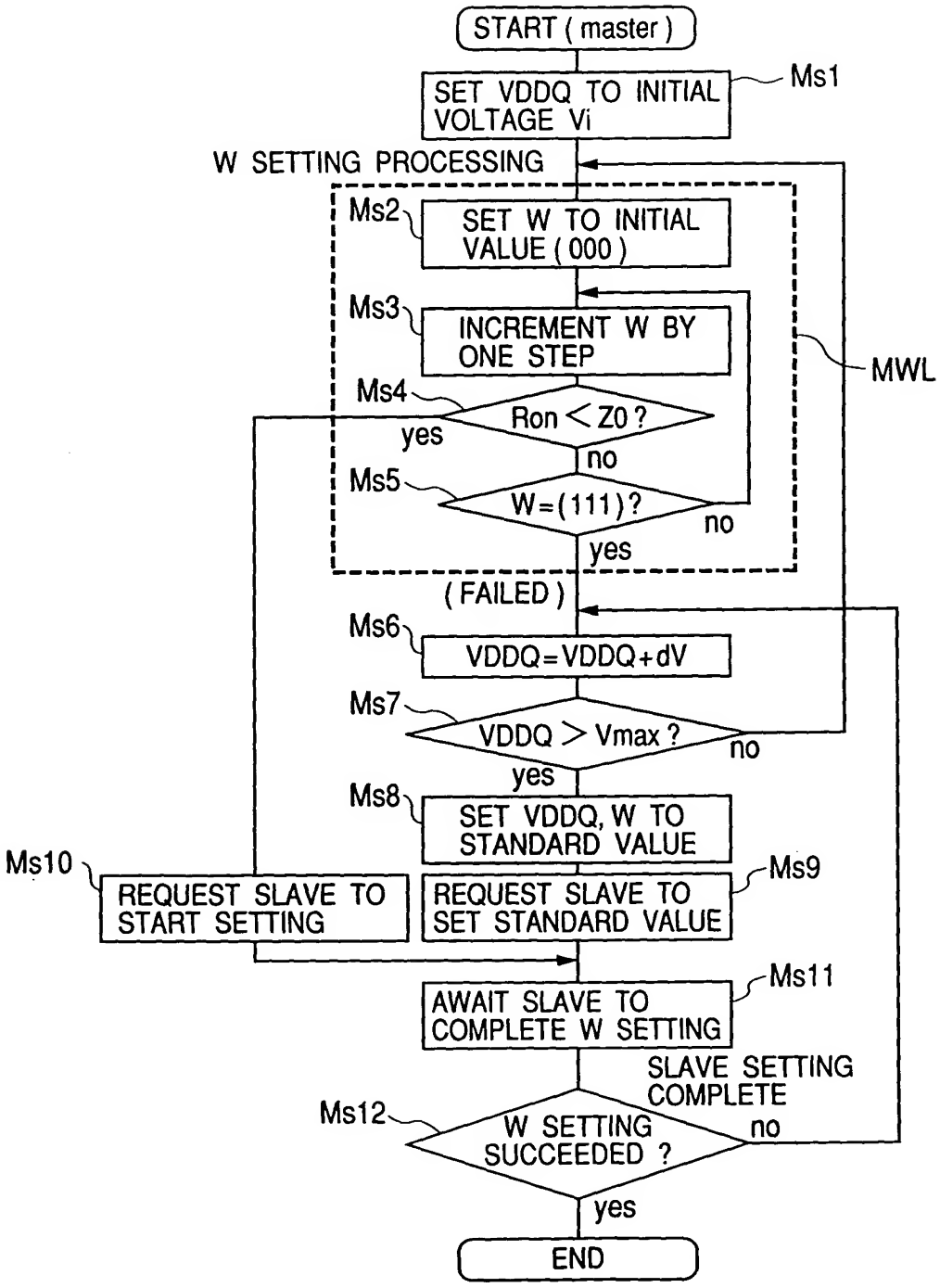

START (master)
SET VDDQ TO INITIAL VOLTAGE Vi
Ms1
W SETTING PROCESSING
Ms2
SET W TO INITIAL VALUE (000)
Ms3
INCREMENT W BY ONE STEP
MWL
Ms4
Ron < Z0 ?
yes
no
Ms5
W=(111)?
no
yes
(FAILED)
Ms6
VDDQ=VDDQ+dV
Ms7
VDDQ > Vmax ?
no
yes
Ms8
SET VDDQ, W TO STANDARD VALUE
Ms10
REQUEST SLAVE TO START SETTING
REQUEST SLAVE TO SET STANDARD VALUE
Ms9
Ms11
AWAIT SLAVE TO COMPLETE W SETTING
SLAVE SETTING COMPLETE
Ms12
W SETTING SUCCEEDED ?
no
yes
END

FIG. 7

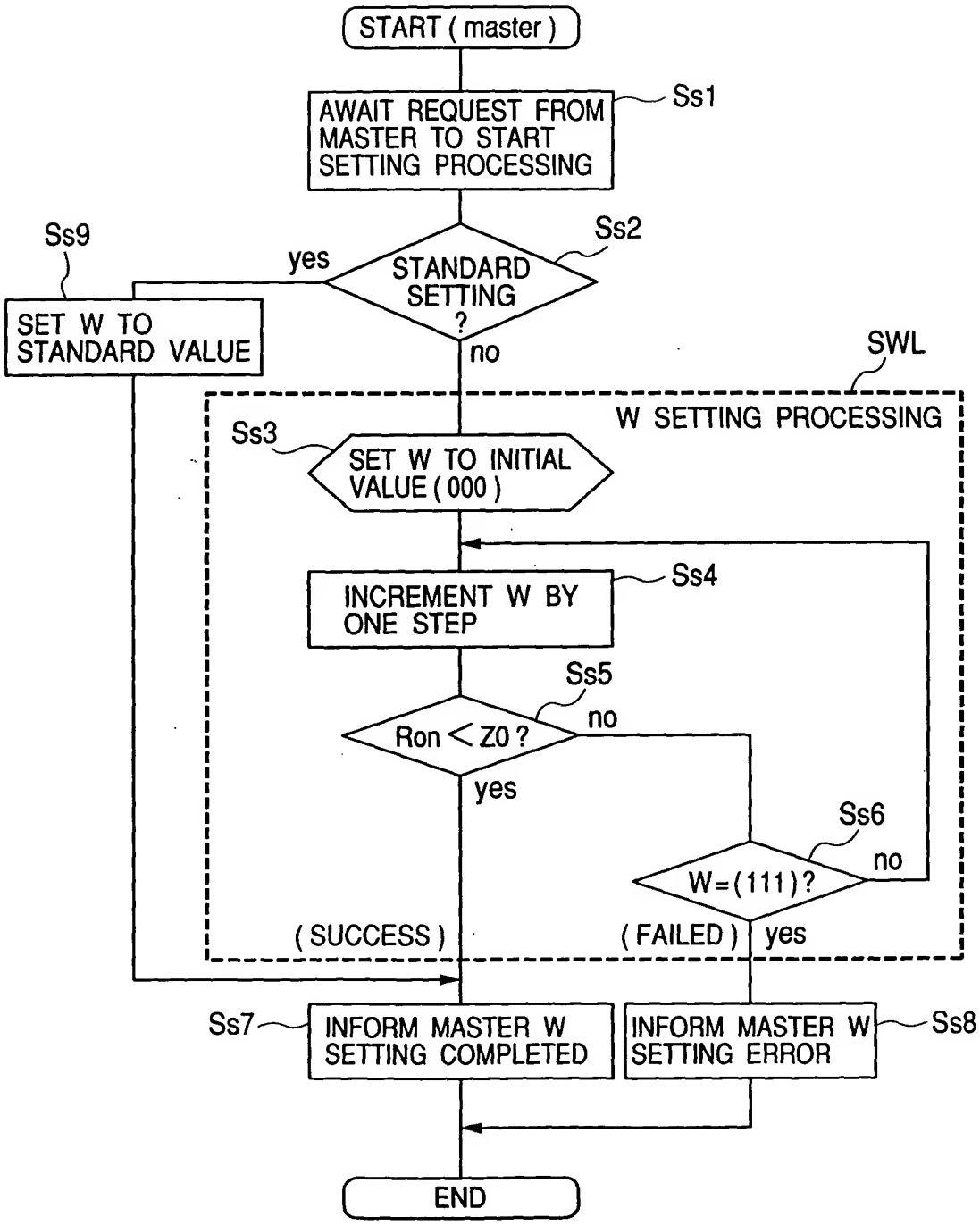

START (master)
AWAIT REQUEST FROM MASTER TO START SETTING PROCESSING
Ss1
STANDARD SETTING ?
Ss2
yes
no
Ss9
SET W TO STANDARD VALUE
SWL
W SETTING PROCESSING
Ss3
SET W TO INITIAL VALUE (000)
INCREMENT W BY ONE STEP
Ss4
Ss5
Ron < Z0 ?
no
yes
Ss6
W=(111)?
no
yes
(SUCCESS)
(FAILED)
Ss7
INFORM MASTER W SETTING COMPLETED
INFORM MASTER W SETTING ERROR
Ss8
END

FIG. 8

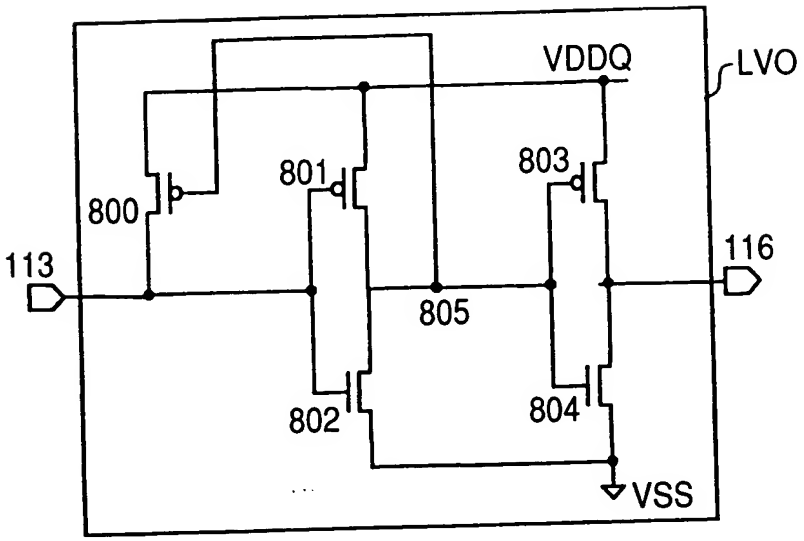

VDDQ
LVO
800
801
803
113
116
805
802
804
VSS

FIG. 9

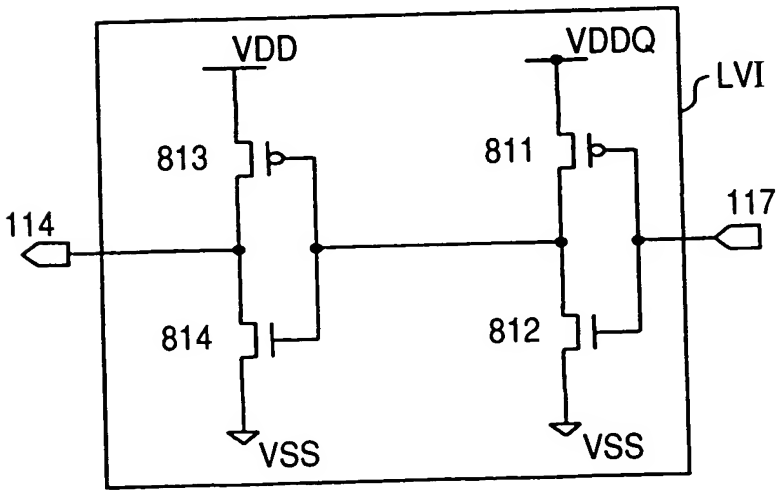

VDD
VDDQ
LVI
813
811
114
117
814
812
VSS
VSS

FIG. 10

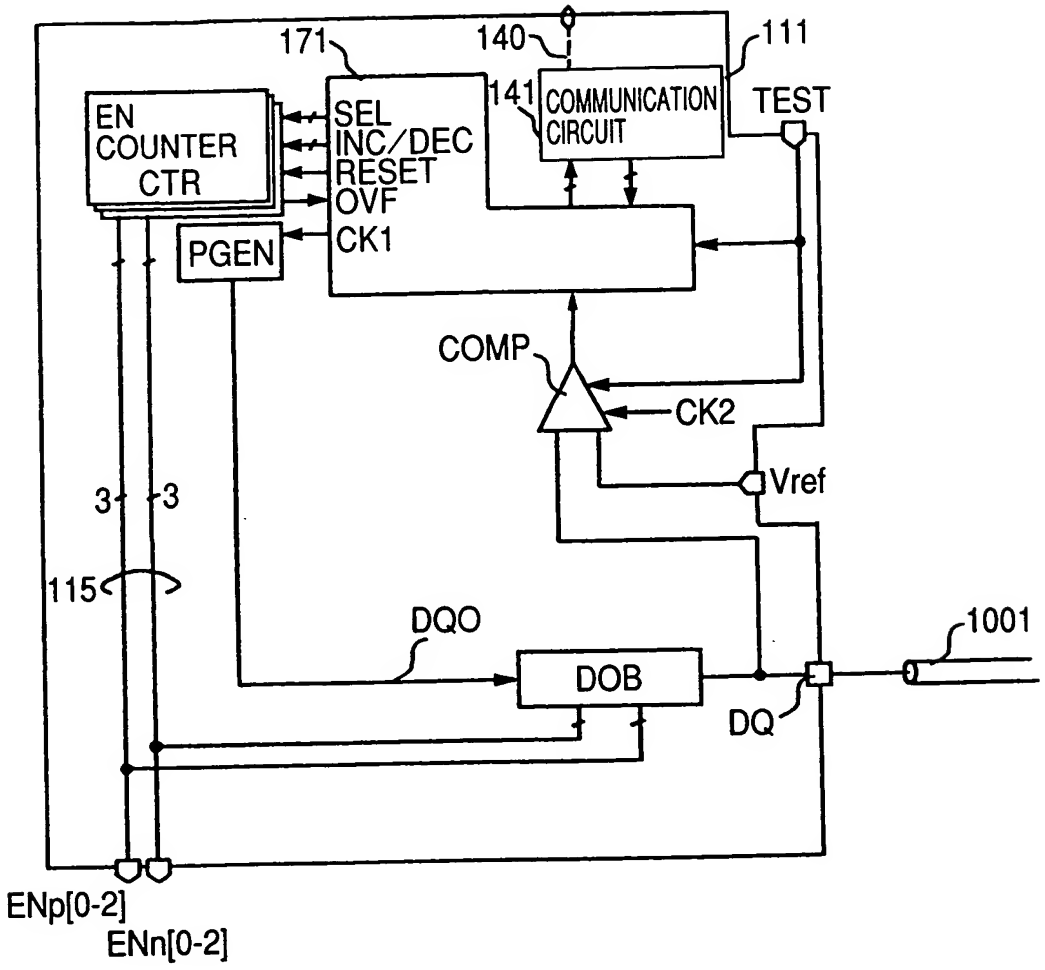

171
140
111
141
COMMUNICATION CIRCUIT
TEST
EN COUNTER CTR
SEL
INC/DEC
RESET
OVF
CK1
PGEN
COMP
CK2
Vref
3
3
115
DQO
1001
DOB
DQ
ENp[0-2]
ENn[0-2]

FIG. 11

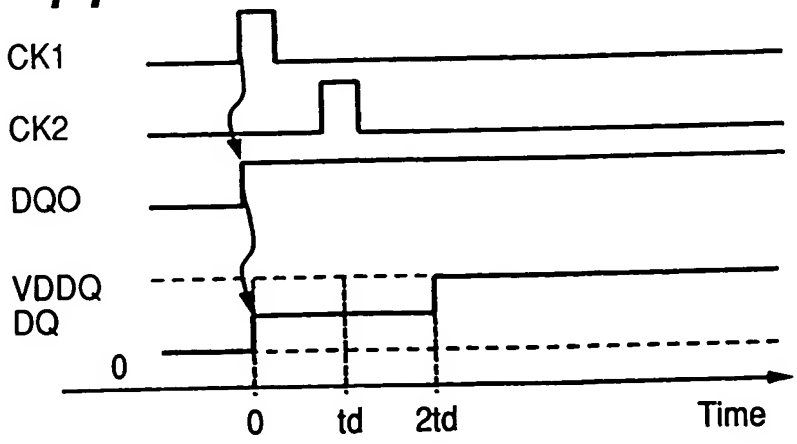

CK1
CK2
DQO
VDDQ
DQ
0
0
td
2td
Time

FIG. 12

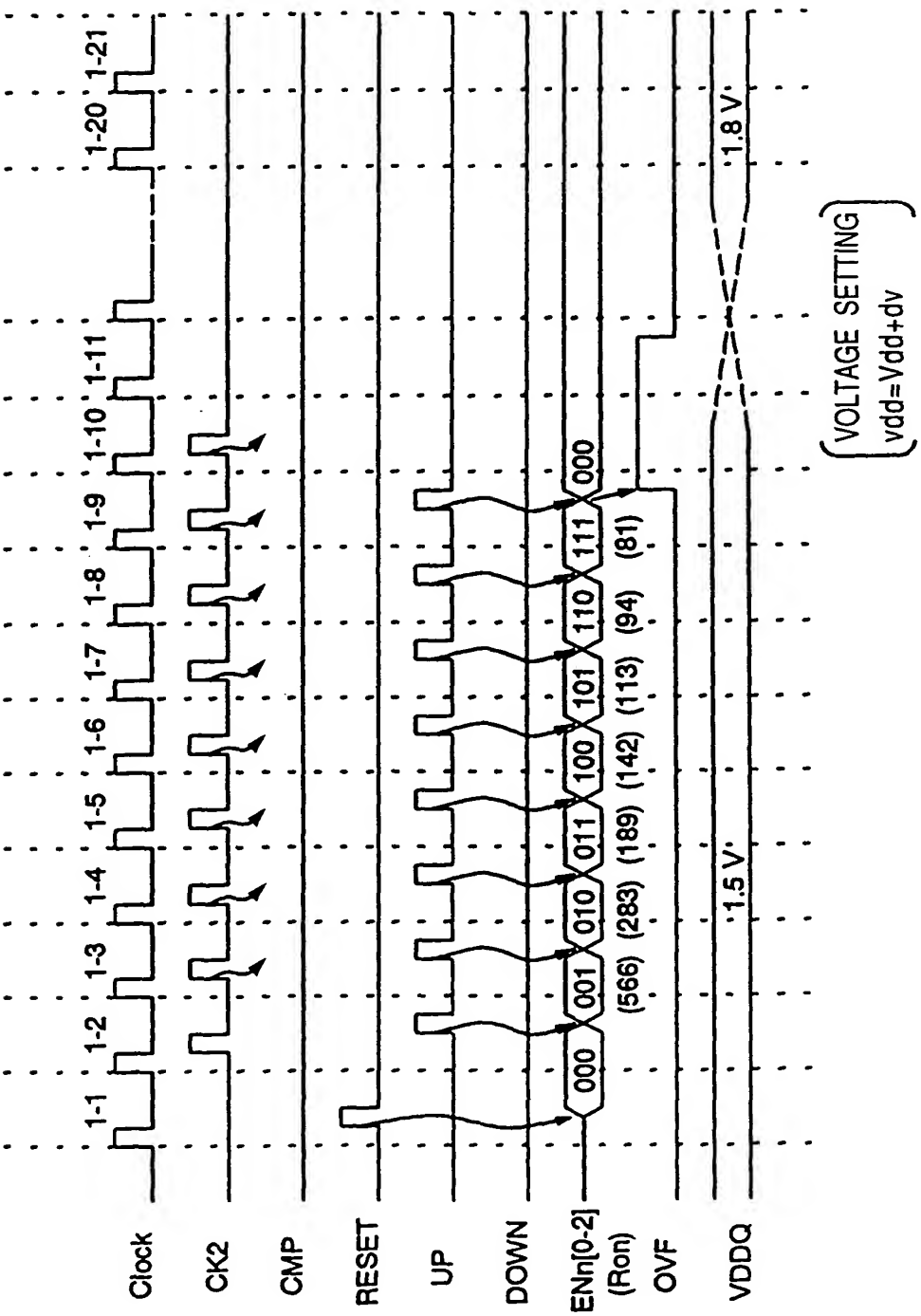

Clock
CK2
CMP
RESET
UP
DOWN
ENn[0-2]
(Ron)
OVF
VDDQ
1-1
1-2
1-3
1-4
1-5
1-6
1-7
1-8
1-9
1-10
1-11
1-20
1-21
000
001
010
011
100
101
110
111
(566)
(283)
(189)
(142)
(113)
(94)
(81)
1.5 V
1.8 V
VOLTAGE SETTING
vdd=Vdd+dv

FIG. 13

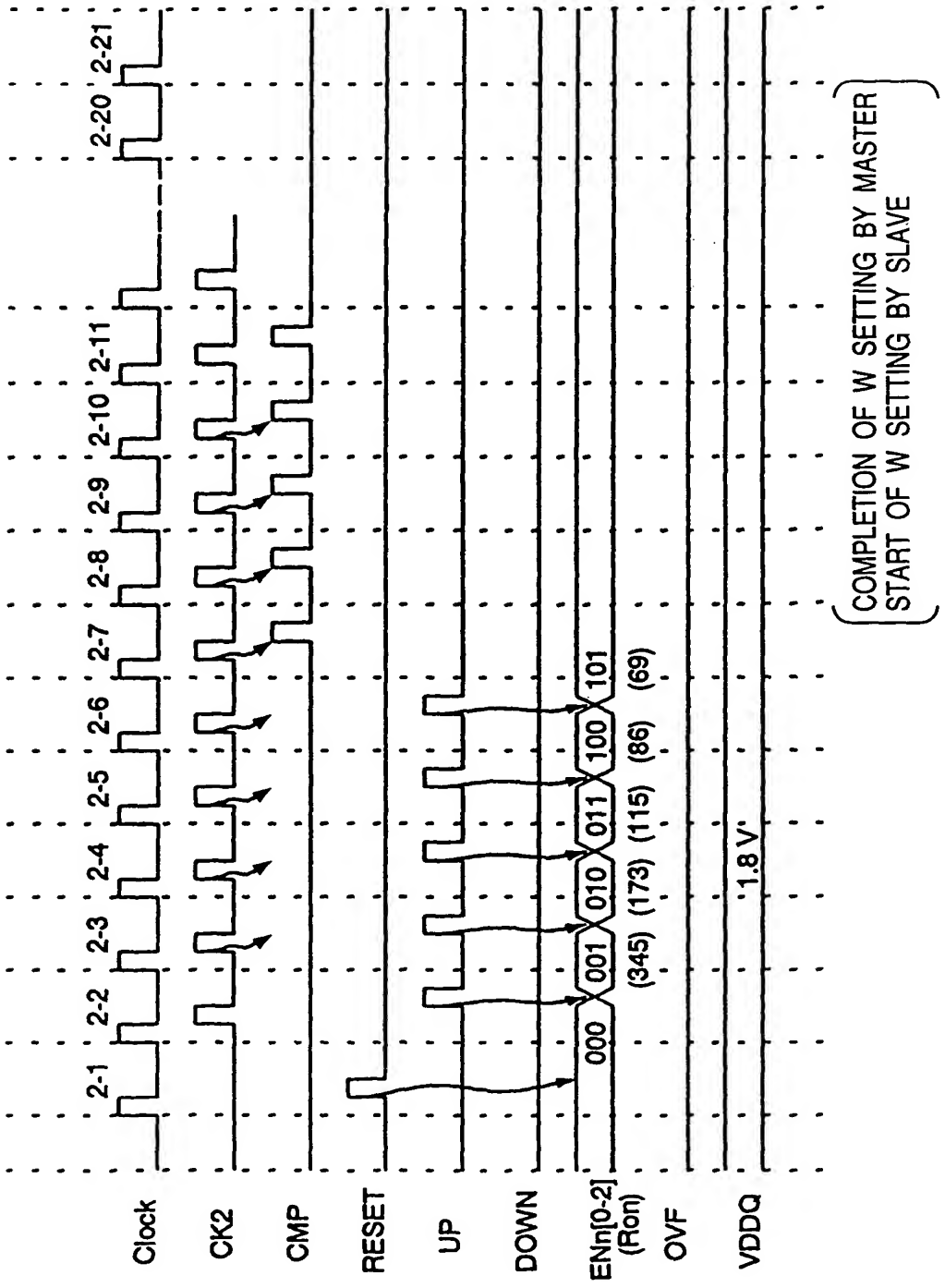

Clock
CK2
CMP
RESET
UP
DOWN
ENn[0-2]
(Ron)
OVF
VDDQ
2-1
2-2
2-3
2-4
2-5
2-6
2-7
2-8
2-9
2-10
2-11
2-20
2-21
000
001
010
011
100
101
(345)
(173)
(115)
(86)
(69)
1.8 V
COMPLETION OF W SETTING BY MASTER
START OF W SETTING BY SLAVE

FIG. 14

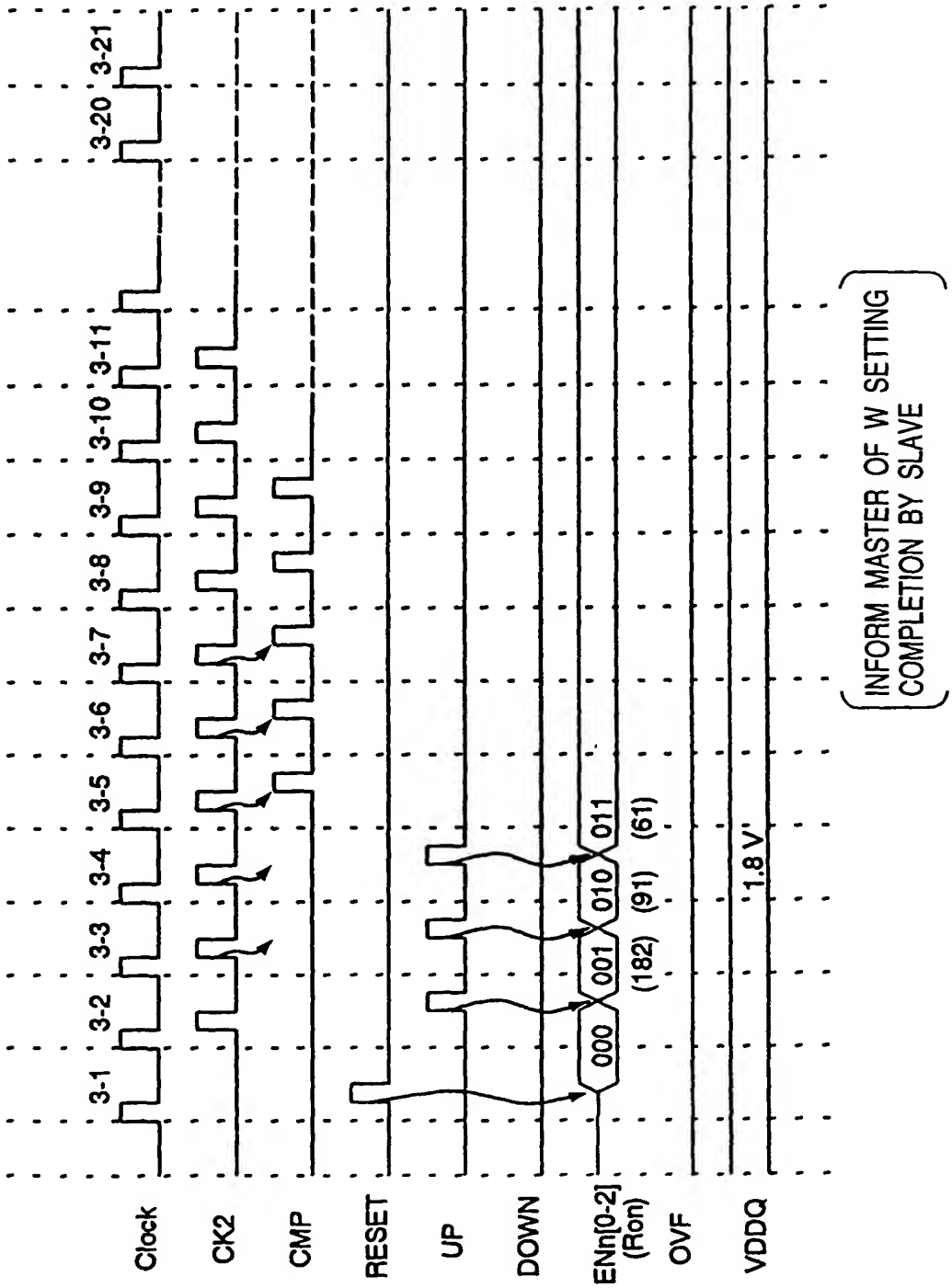

3-1
3-2
3-3
3-4
3-5
3-6
3-7
3-8
3-9
3-10
3-11
3-20
3-21
Clock
CK2
CMP
RESET
UP
DOWN
ENn[0-2]
(Ron)
OVF
VDDQ
000
001
010
011
(182)
(91)
(61)
1.8 V
INFORM MASTER OF W SETTING
COMPLETION BY SLAVE

FIG. 15

To	From	What	CODE to	CODE from	CODE what
All	Master	START ALL SETTING MODES	000	100	0000
All	Master	COMPLETE ALL SETTING MODES	000	100	0001
VGEN	Master	REQUEST VOLTAGE SETTING (UP)	111	100	0010
VGEN	Master	REQUEST VOLTAGE SETTING (DOWN)	111	100	0011
Master	VGEN	COMPLETE VOLTAGE SETTING	100	111	0100
Slave	Master	REQUEST TO START W SETTING	id	100	0101
Slave	Master	REQUEST TO SET W STANDARD VALUE	id	100	0110
Master	Slave	COMPLETE W SETTING (SUCCEEDED)	100	id	0111
Master	Slave	COMPLETE W SETTING (FAILED)	100	id	1000

FIG. 16

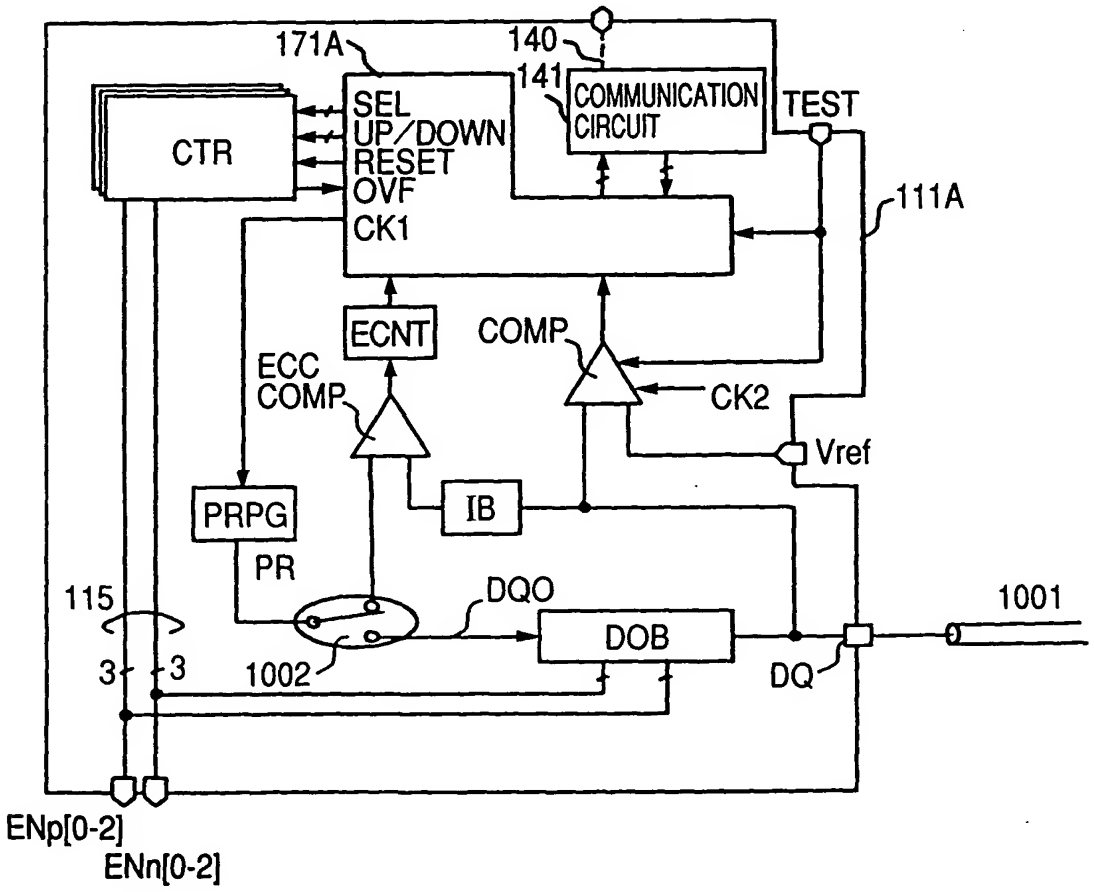


FIG. 17

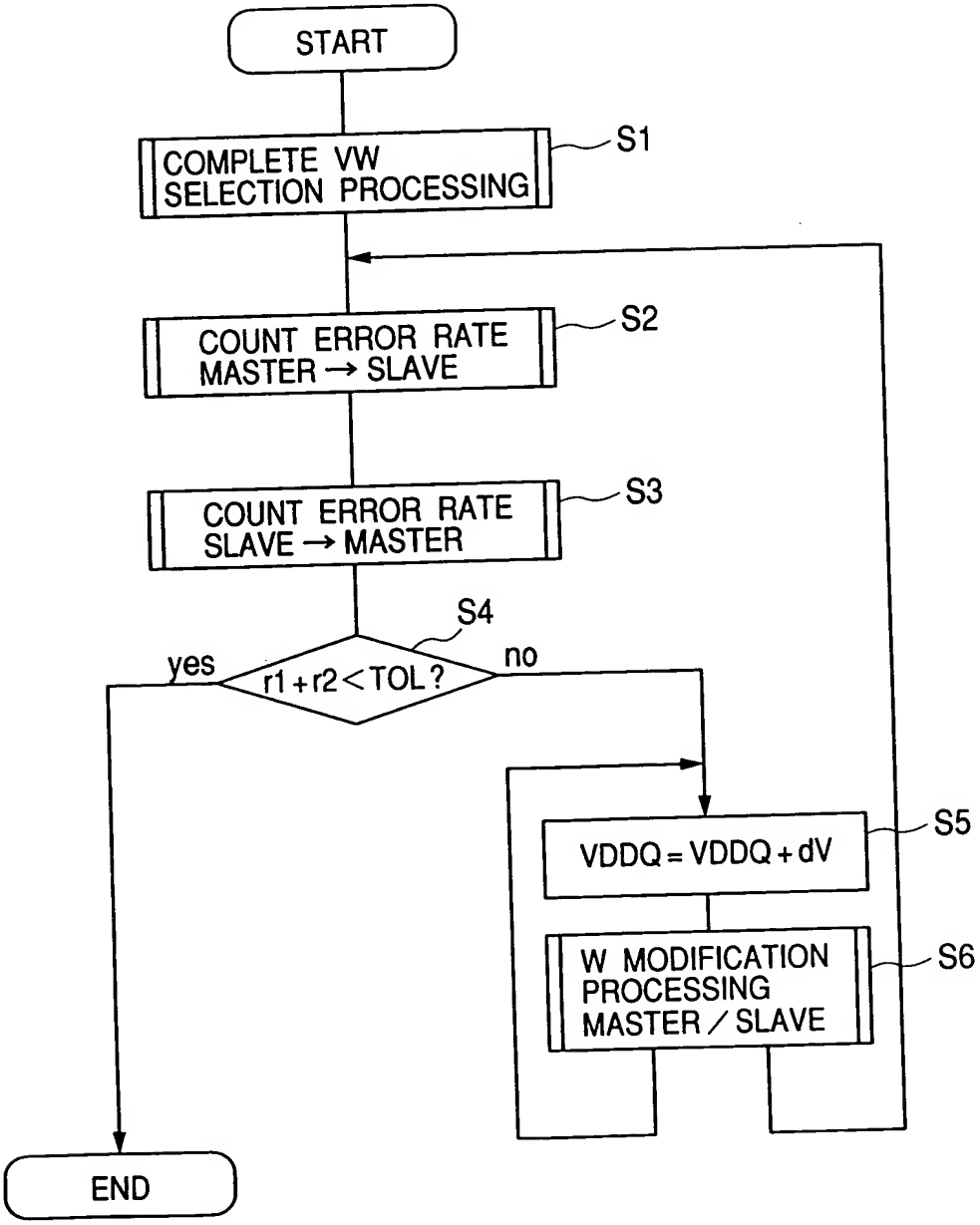

START
COMPLETE VW SELECTION PROCESSING
S1
COUNT ERROR RATE MASTER → SLAVE
S2
COUNT ERROR RATE SLAVE → MASTER
S3
S4
r1+r2<TOL?
yes
no
VDDQ=VDDQ+dV
S5
W MODIFICATION PROCESSING MASTER / SLAVE
S6
END

FIG. 18

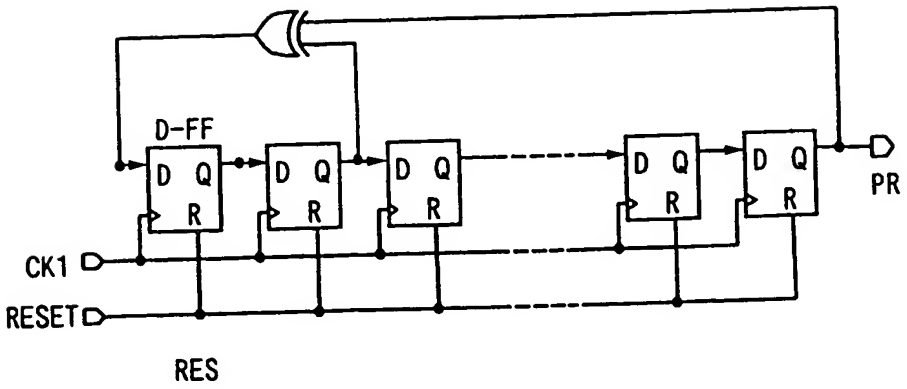

D-FF
D Q
R
PR
CK1
RESET
RES

FIG. 19

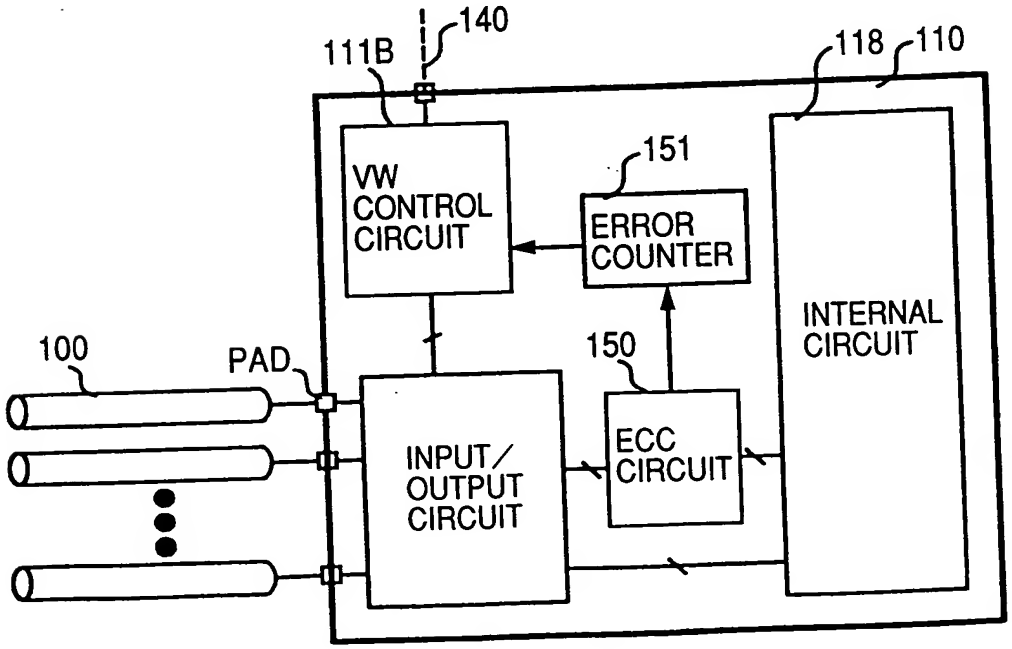

140
111B
118
110
VW
CONTROL
CIRCUIT
151
ERROR
COUNTER
INTERNAL
CIRCUIT
100
PAD
150
INPUT/
OUTPUT
CIRCUIT
ECC
CIRCUIT

FIG. 20

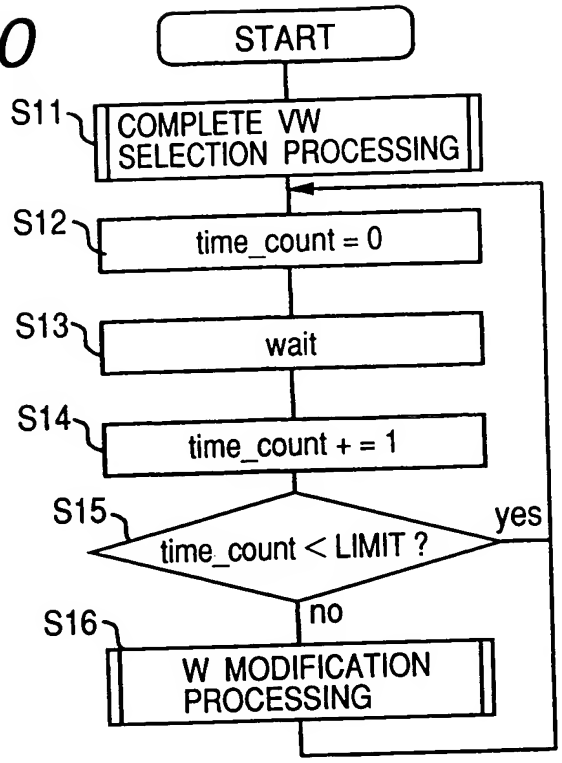

START
S11
COMPLETE VW SELECTION PROCESSING
S12
time_count = 0
S13
wait
S14
time_count + = 1
S15
time_count < LIMIT ?
yes
no
S16
W MODIFICATION PROCESSING

FIG. 21

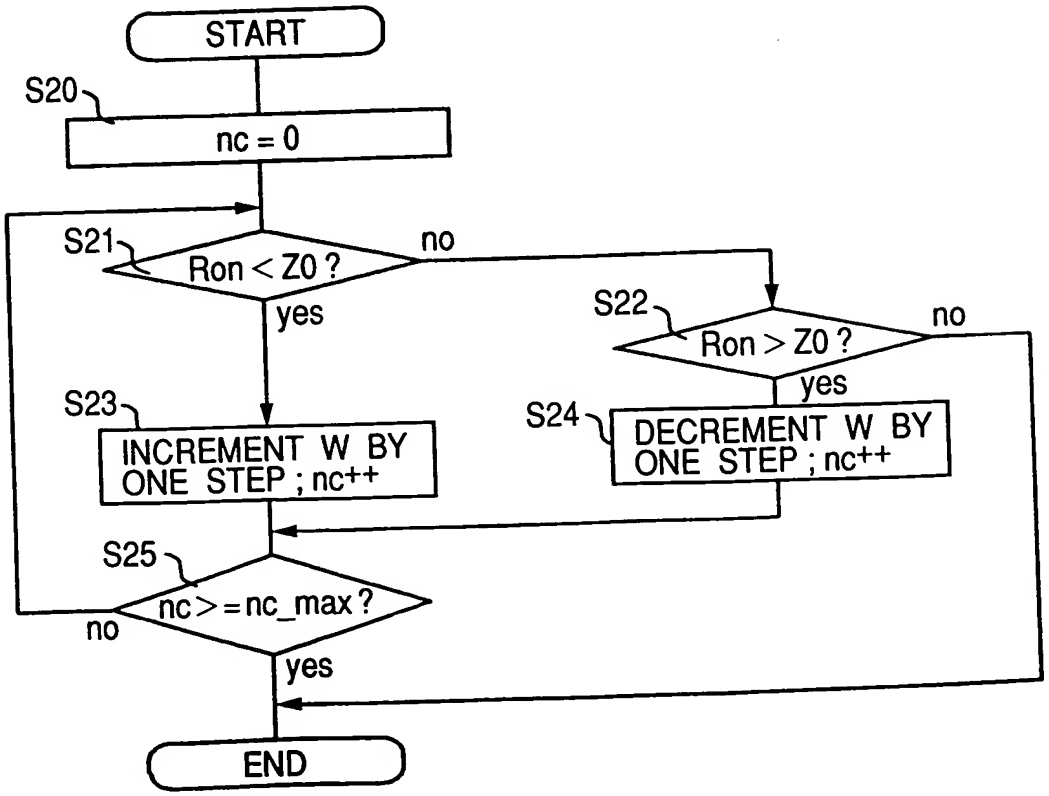

START
S20
nc = 0
S21
Ron < Z0 ?
no
yes
S22
Ron > Z0 ?
no
yes
S23
INCREMENT W BY ONE STEP ; nc++
S24
DECREMENT W BY ONE STEP ; nc++
S25
nc > = nc_max ?
no
yes
END

FIG. 22

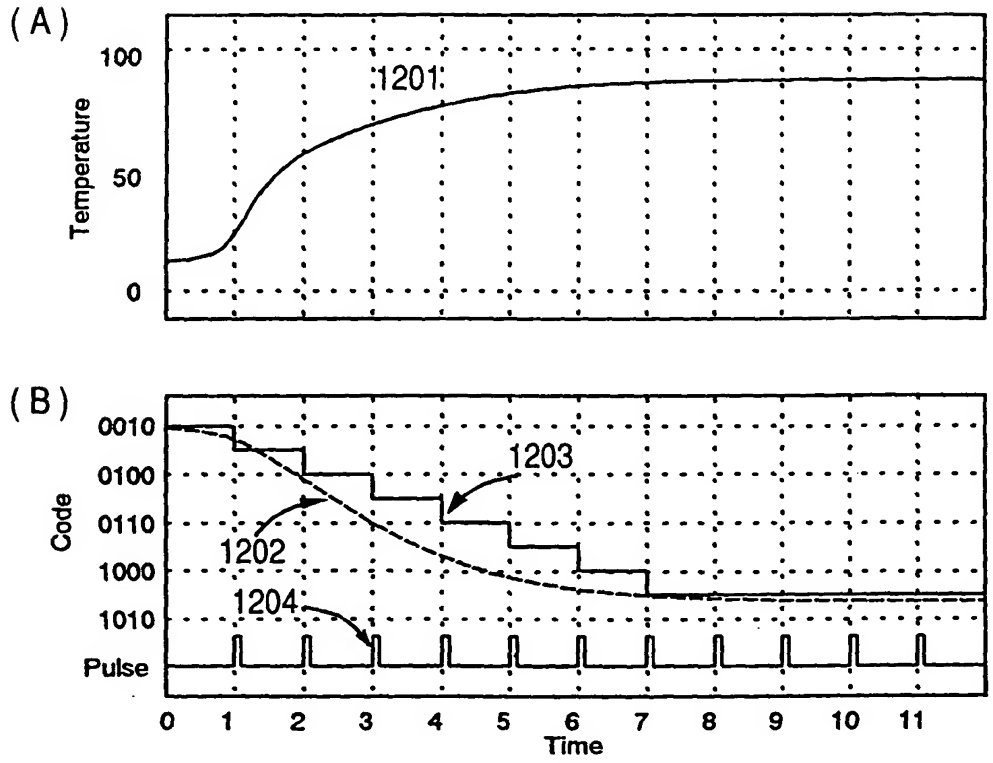

(A)
100
50
0
Temperature
1201
(B)
0010
0100
0110
1000
1010
Pulse
Code
1202
1203
1204
0 1 2 3 4 5 6 7 8 9 10 11
Time

FIG. 23

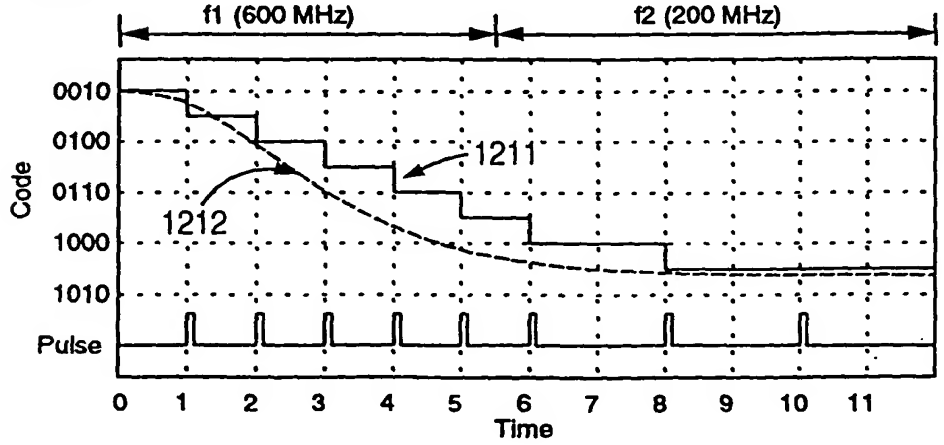

f1 (600 MHz)
f2 (200 MHz)
0010
0100
0110
1000
1010
Pulse
Code
1211
1212
0 1 2 3 4 5 6 7 8 9 10 11
Time

FIG. 24

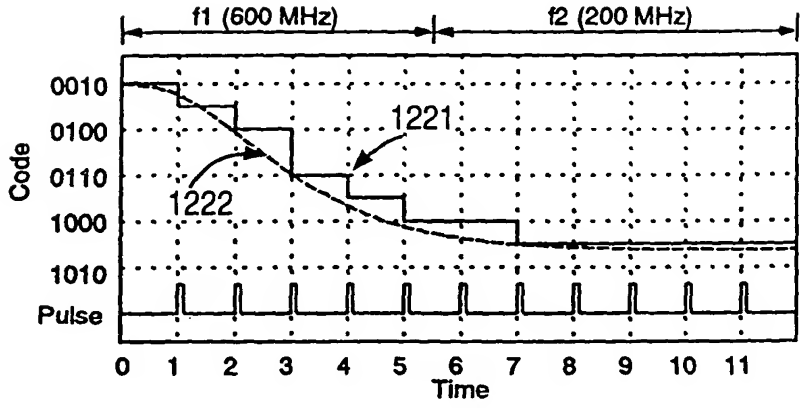

f1 (600 MHz)
f2 (200 MHz)
0010
0100
0110
1000
1010
Pulse
Code
1221
1222
0 1 2 3 4 5 6 7 8 9 10 11
Time

FIG. 25

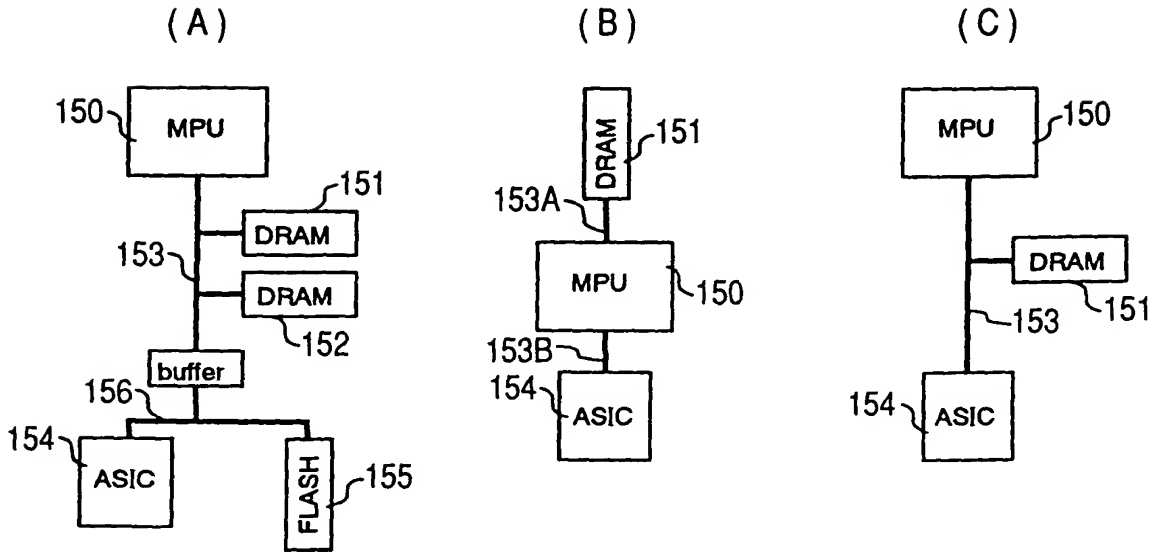

(A)
150
MPU
151
DRAM
153
DRAM
152
buffer
156
154
ASIC
FLASH
155
(B)
DRAM
151
153A
MPU
150
153B
154
ASIC
(C)
MPU
150
DRAM
151
153
154
ASIC

FIG. 26

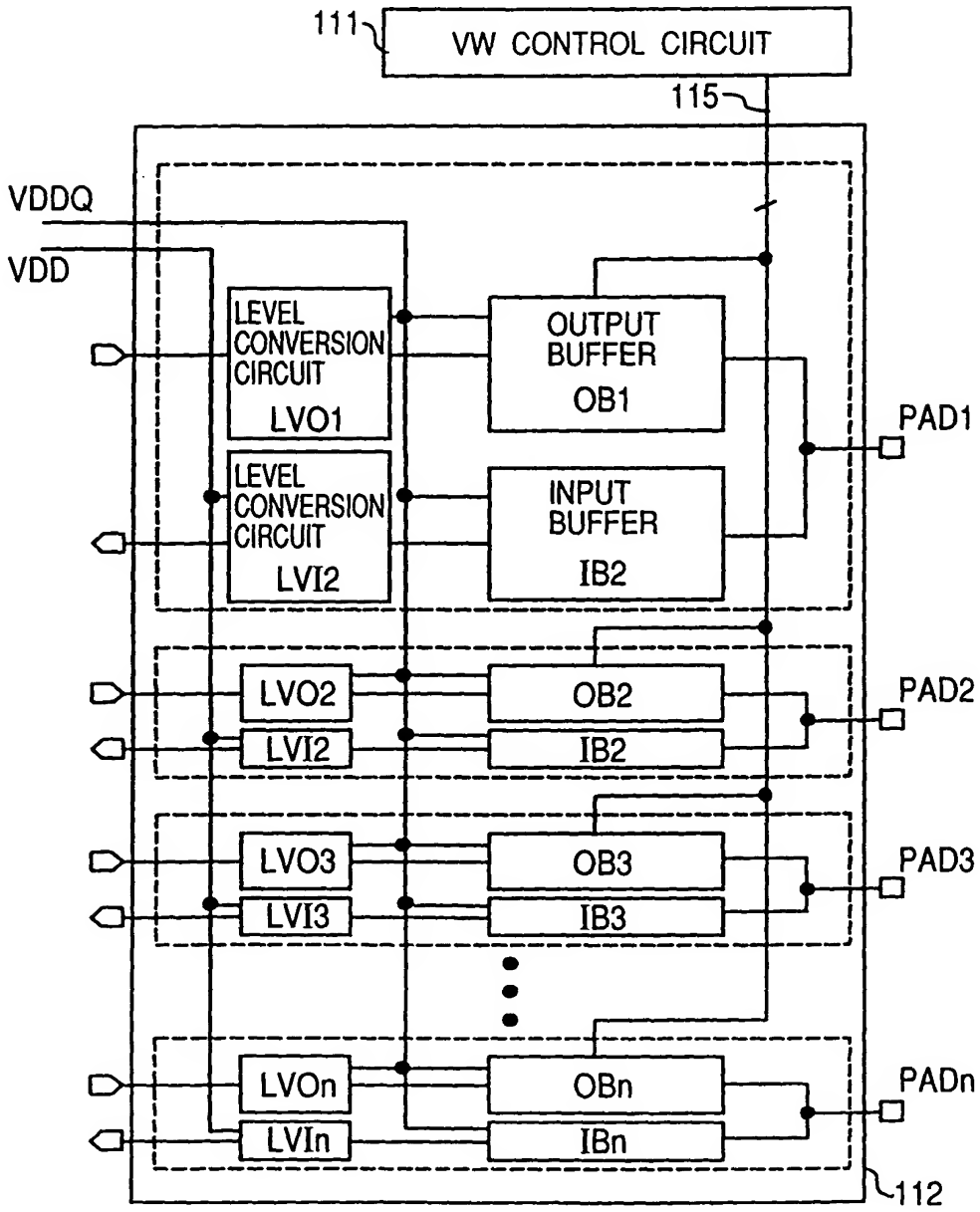
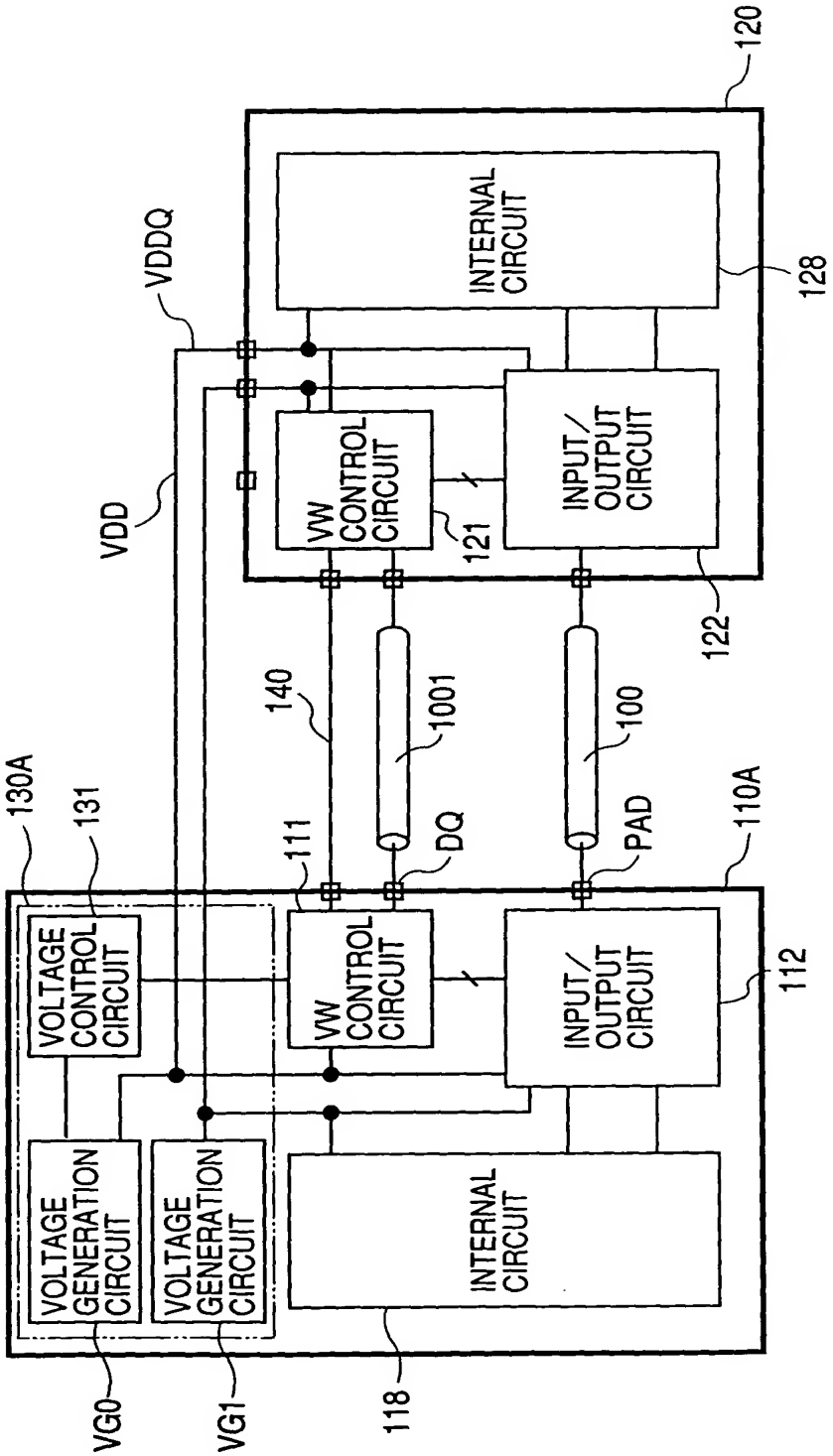

111
VW CONTROL CIRCUIT
115
VDDQ
VDD
LEVEL CONVERSION CIRCUIT
LVO1
OUTPUT BUFFER
OB1
PAD1
LEVEL CONVERSION CIRCUIT
LVI2
INPUT BUFFER
IB2
LVO2
OB2
PAD2
LVI2
IB2
LVO3
OB3
PAD3
LVI3
IB3
LVOn
OBn
PADn
LVIn
IBn
112

FIG. 27


120
INTERNAL CIRCUIT
128
VDDQ
VDD
VW CONTROL CIRCUIT
121
INPUT/ OUTPUT CIRCUIT
122
140
1001
100
130A
131
111
DQ
PAD
110A
VOLTAGE CONTROL CIRCUIT
VW CONTROL CIRCUIT
INPUT/ OUTPUT CIRCUIT
112
VOLTAGE GENERATION CIRCUIT
VOLTAGE GENERATION CIRCUIT
INTERNAL CIRCUIT
VG0
VG1
118

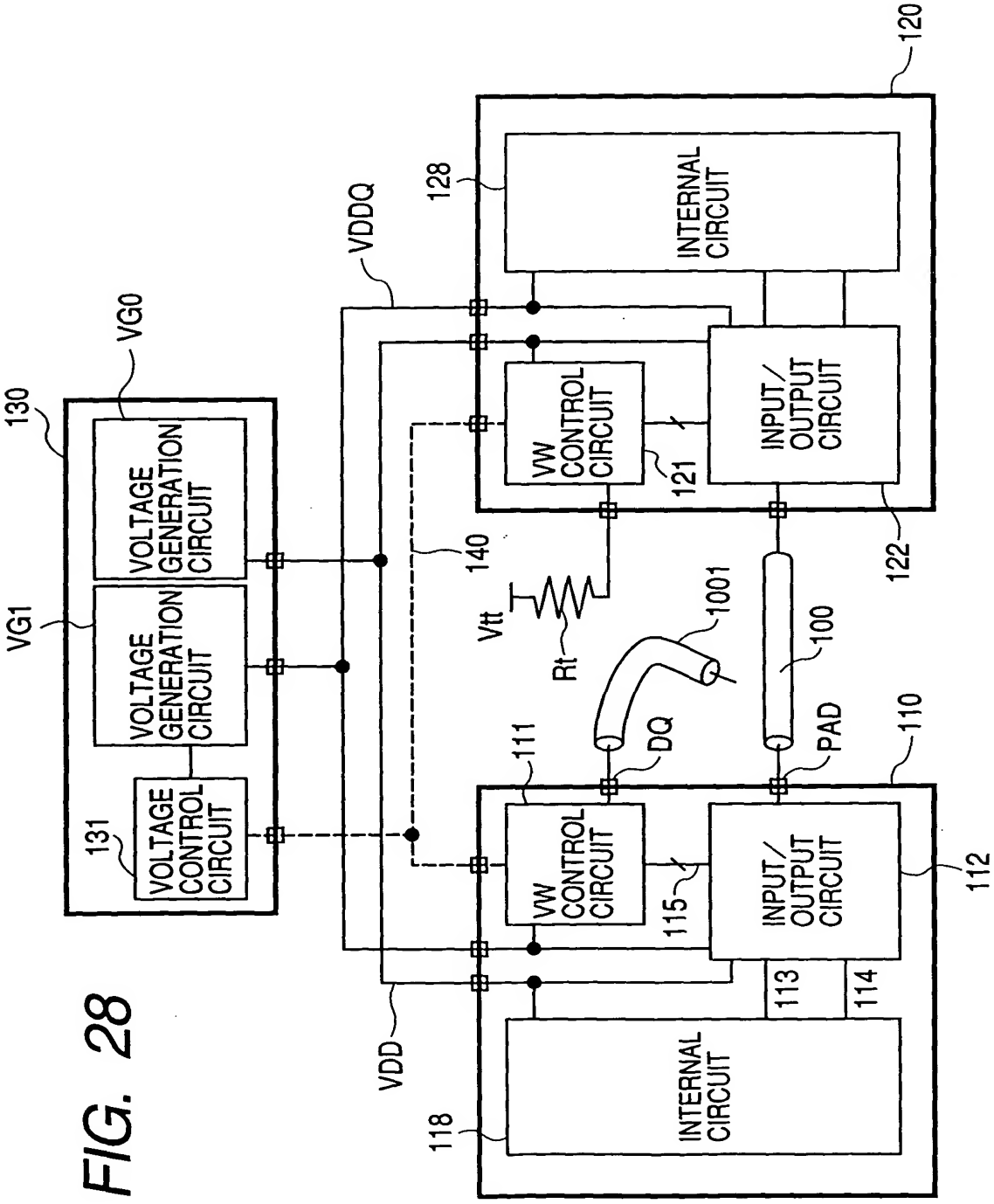

120
128
INTERNAL CIRCUIT
VDDQ
VG0
130
VOLTAGE GENERATION CIRCUIT
VG1
VOLTAGE GENERATION CIRCUIT
131
VOLTAGE CONTROL CIRCUIT
VW CONTROL CIRCUIT
121
INPUT/ OUTPUT CIRCUIT
122
140
Vtt
Rt
1001
100
DQ
PAD
111
110
VW CONTROL CIRCUIT
115
INPUT/ OUTPUT CIRCUIT
112
113
114
VDD
INTERNAL CIRCUIT
118

FIG. 28

FIG. 29

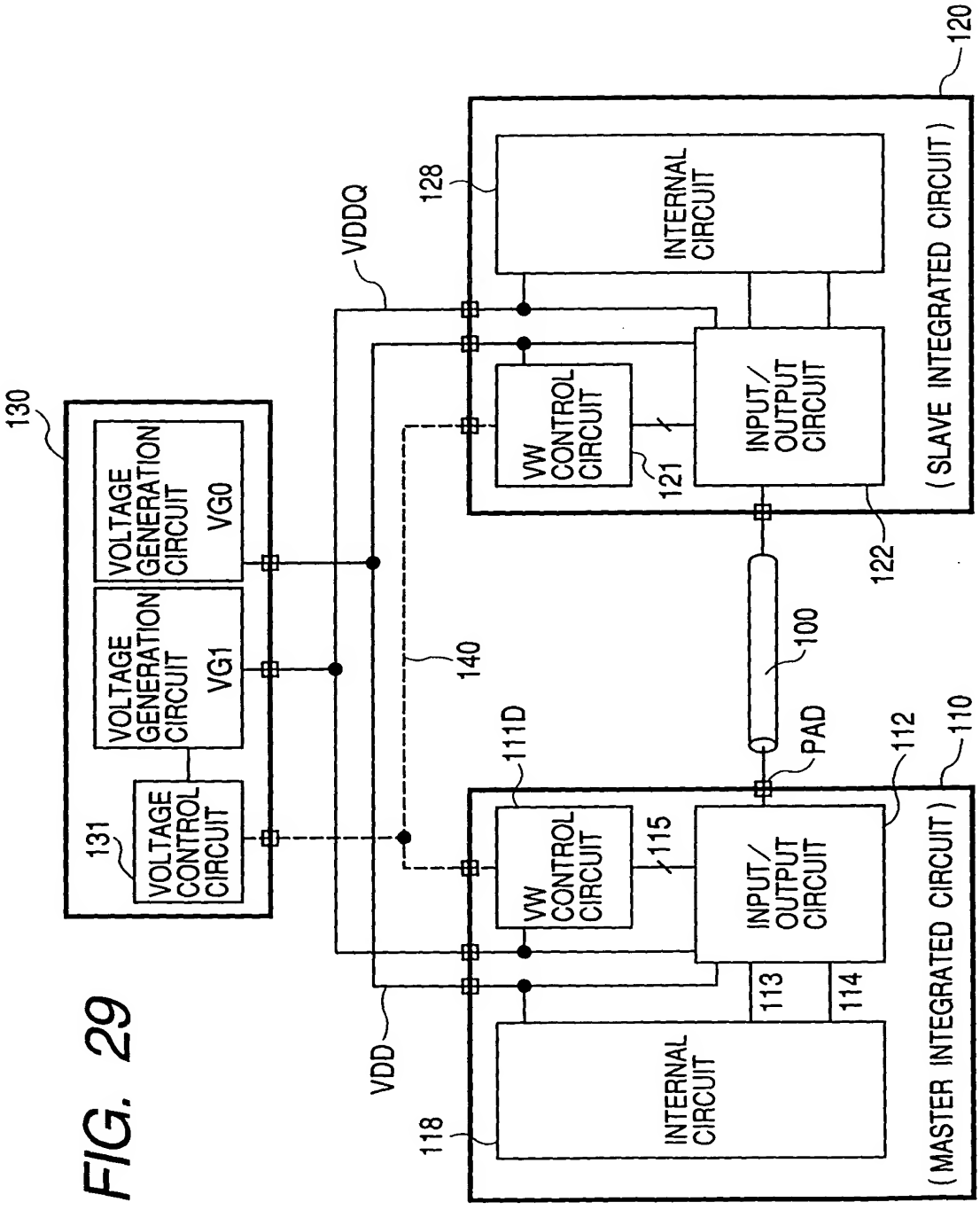

130
VOLTAGE GENERATION CIRCUIT VG0
VOLTAGE GENERATION CIRCUIT VG1
131
VOLTAGE CONTROL CIRCUIT
VDDQ
VDD
140
128
INTERNAL CIRCUIT
VW CONTROL CIRCUIT
121
INPUT/ OUTPUT CIRCUIT
(SLAVE INTEGRATED CIRCUIT)
120
122
100
PAD
111D
112
110
115
113
114
118
(MASTER INTEGRATED CIRCUIT)

FIG. 30

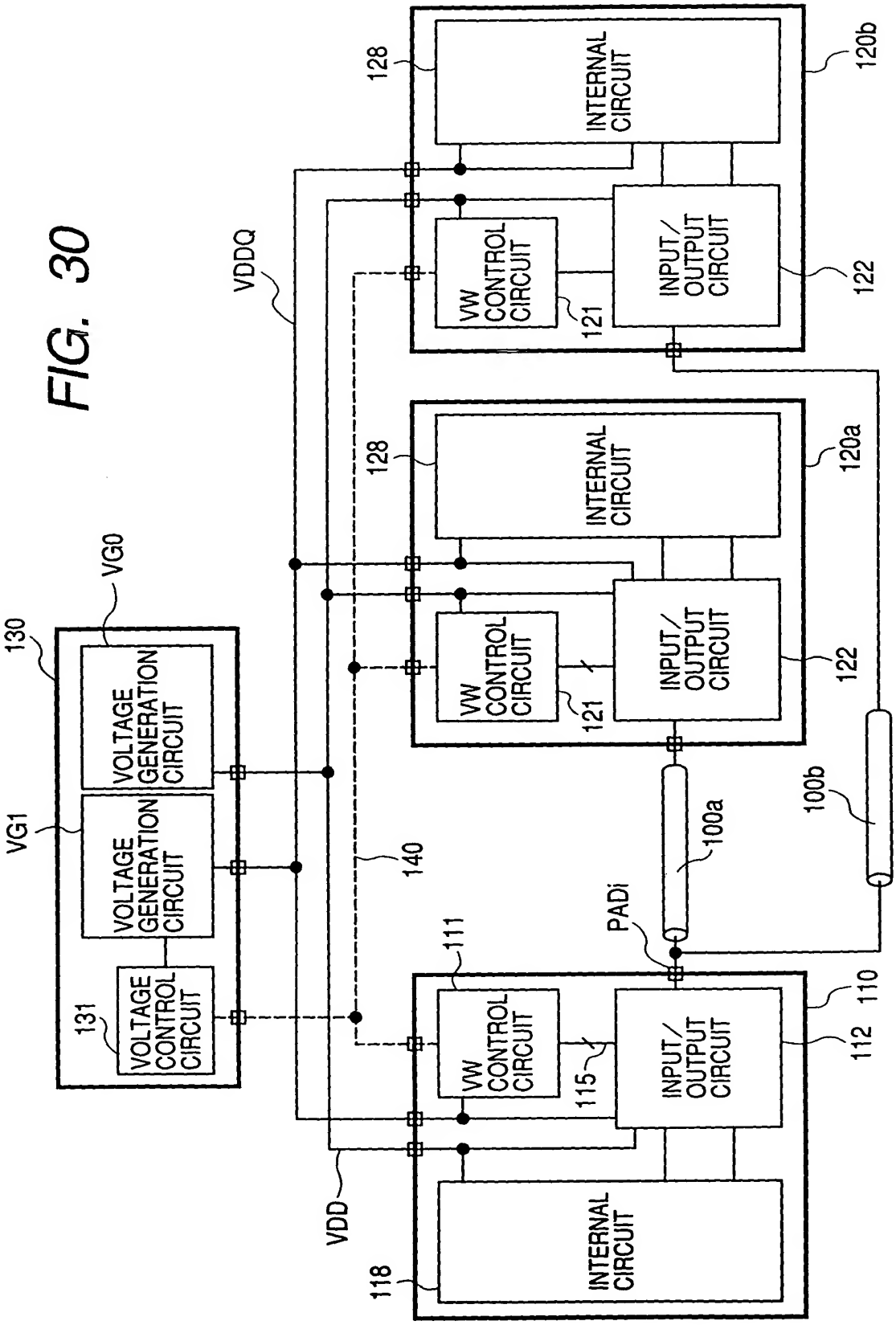

VOLTAGE GENERATION CIRCUIT
VOLTAGE GENERATION CIRCUIT
VOLTAGE CONTROL CIRCUIT
VG0
VG1
130
131
VDDQ
VDD
140
INTERNAL CIRCUIT
VW CONTROL CIRCUIT
INPUT/OUTPUT CIRCUIT
128
120b
120a
122
121
100a
100b
PADi
111
110
112
115
118

FIG. 31

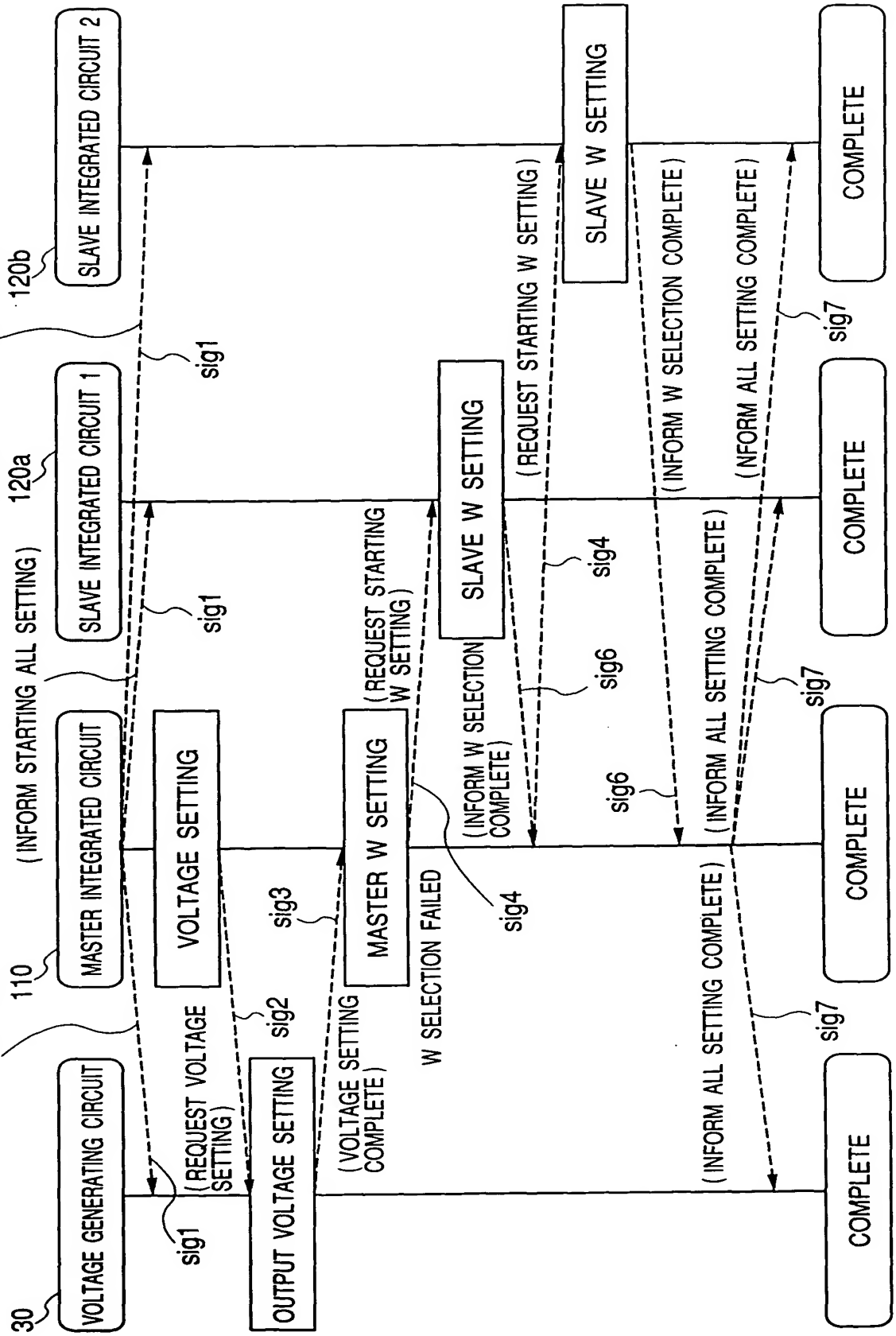

(INFORM STARTING ALL SETTING)
130
VOLTAGE GENERATING CIRCUIT
110
MASTER INTEGRATED CIRCUIT
120a
SLAVE INTEGRATED CIRCUIT 1
120b
SLAVE INTEGRATED CIRCUIT 2
sig1
(REQUEST VOLTAGE SETTING)
OUTPUT VOLTAGE SETTING
sig2
VOLTAGE SETTING
sig3
(VOLTAGE SETTING COMPLETE)
MASTER W SETTING
W SELECTION FAILED
(REQUEST STARTING W SETTING)
sig4
SLAVE W SETTING
(INFORM W SELECTION COMPLETE)
sig6
(INFORM ALL SETTING COMPLETE)
sig7
COMPLETE

FIG. 32

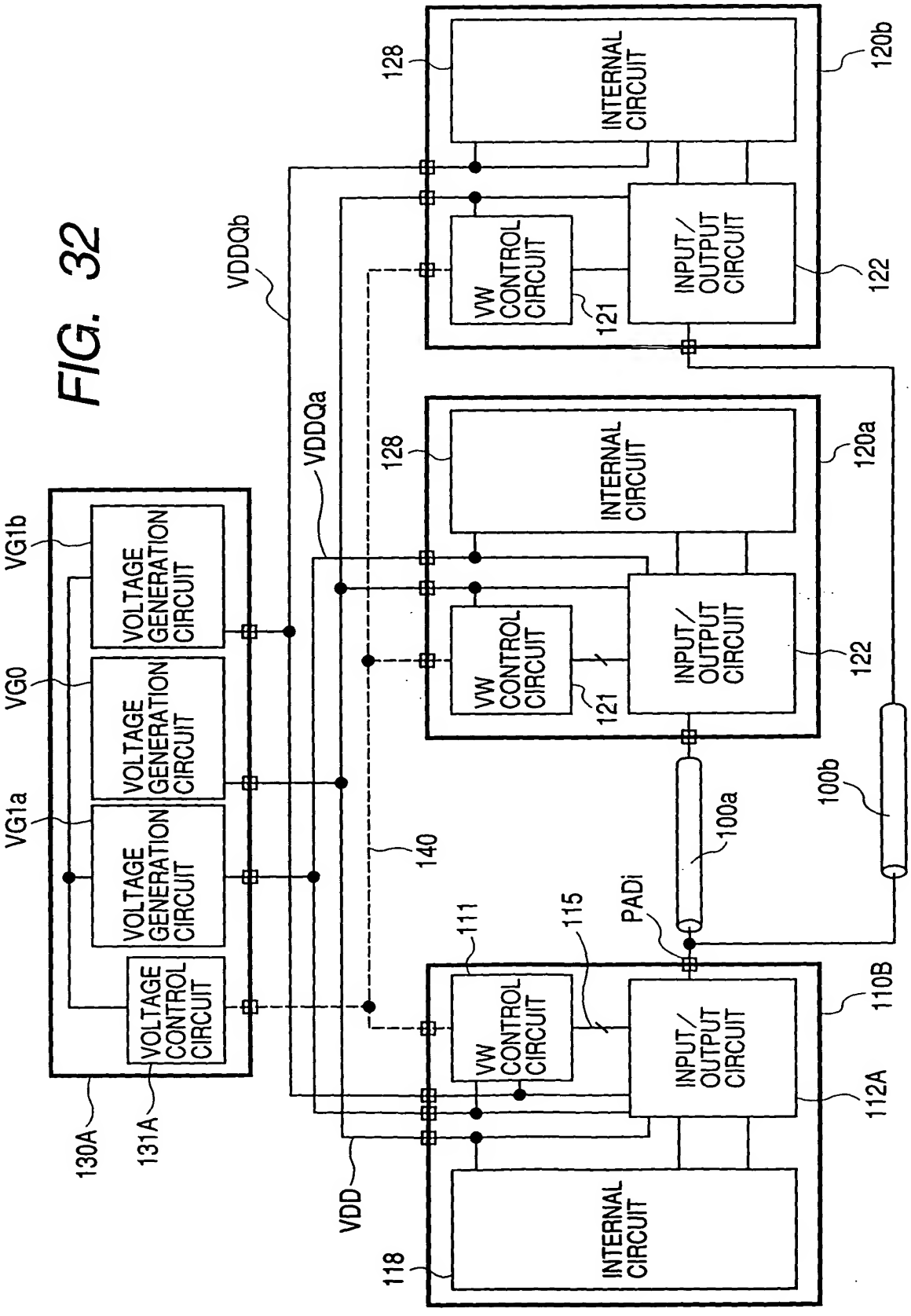

VOLTAGE GENERATION CIRCUIT
VOLTAGE GENERATION CIRCUIT
VOLTAGE GENERATION CIRCUIT
VOLTAGE CONTROL CIRCUIT
VG1b
VG0
VG1a
130A
131A
VDDQb
VDDQa
VDD
140
INTERNAL CIRCUIT
VW CONTROL CIRCUIT
INPUT/ OUTPUT CIRCUIT
128
120b
122
121
120a
100a
100b
PADi
111
115
110B
112A
118

FIG. 33

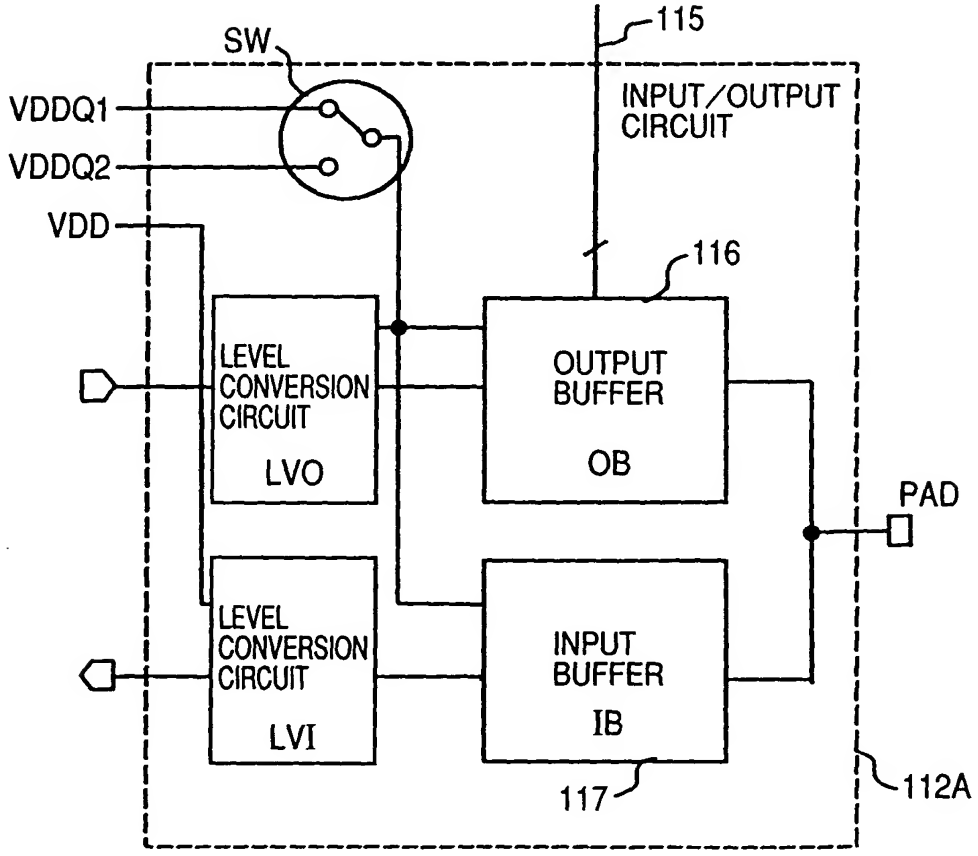

SW
115
VDDQ1
VDDQ2
VDD
INPUT/OUTPUT
CIRCUIT
116
LEVEL
CONVERSION
CIRCUIT
LVO
OUTPUT
BUFFER
OB
PAD
LEVEL
CONVERSION
CIRCUIT
LVI
INPUT
BUFFER
IB
117
112A

FIG. 34

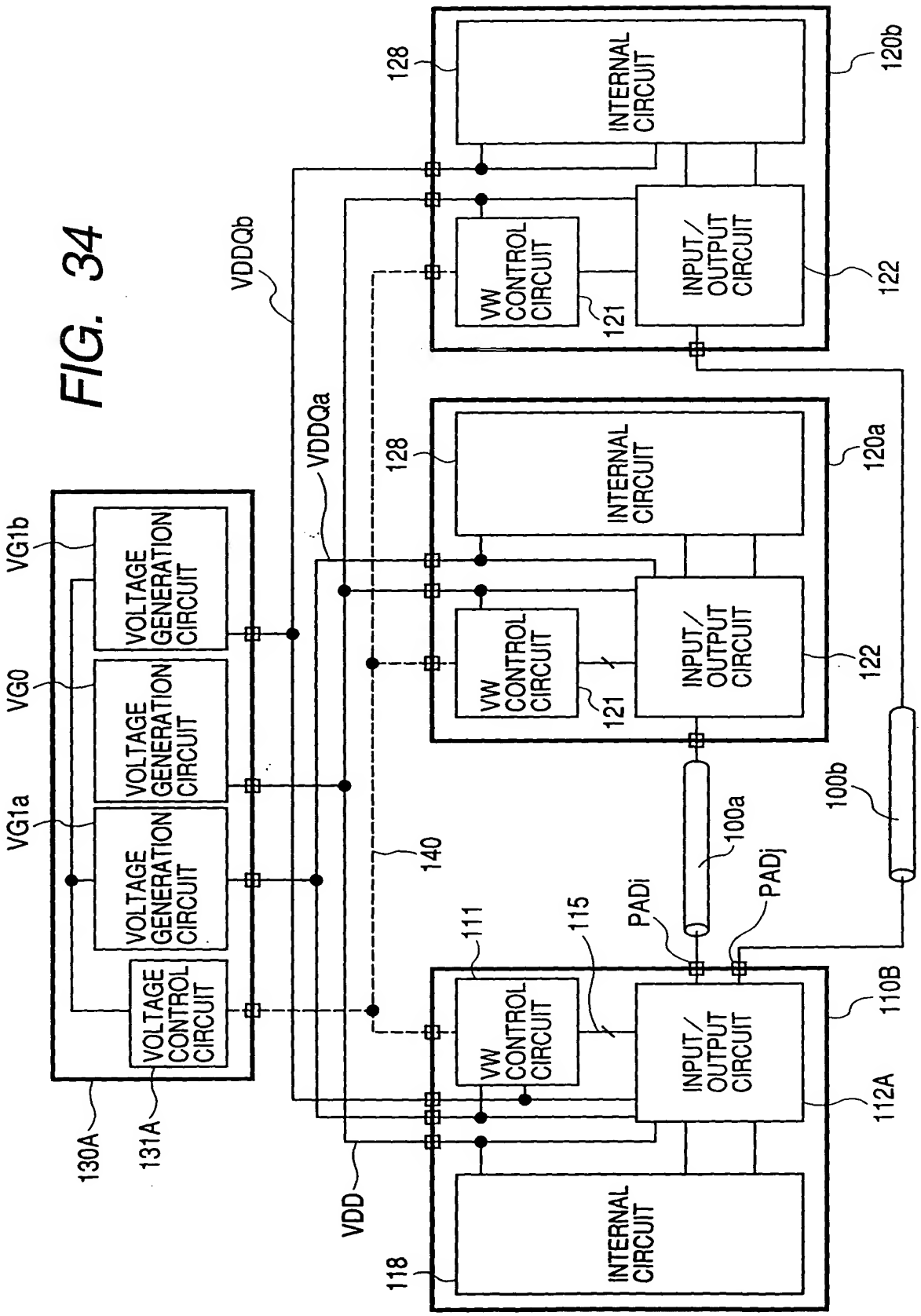

VOLTAGE GENERATION CIRCUIT
VOLTAGE GENERATION CIRCUIT
VOLTAGE GENERATION CIRCUIT
VOLTAGE CONTROL CIRCUIT
VG1b
VG0
VG1a
130A
131A
VDDQb
VDDQa
VDD
140
INTERNAL CIRCUIT
VW CONTROL CIRCUIT
INPUT/ OUTPUT CIRCUIT
128
120b
122
121
120a
100a
100b
PADi
PADj
111
115
110B
112A
118

FIG. 35

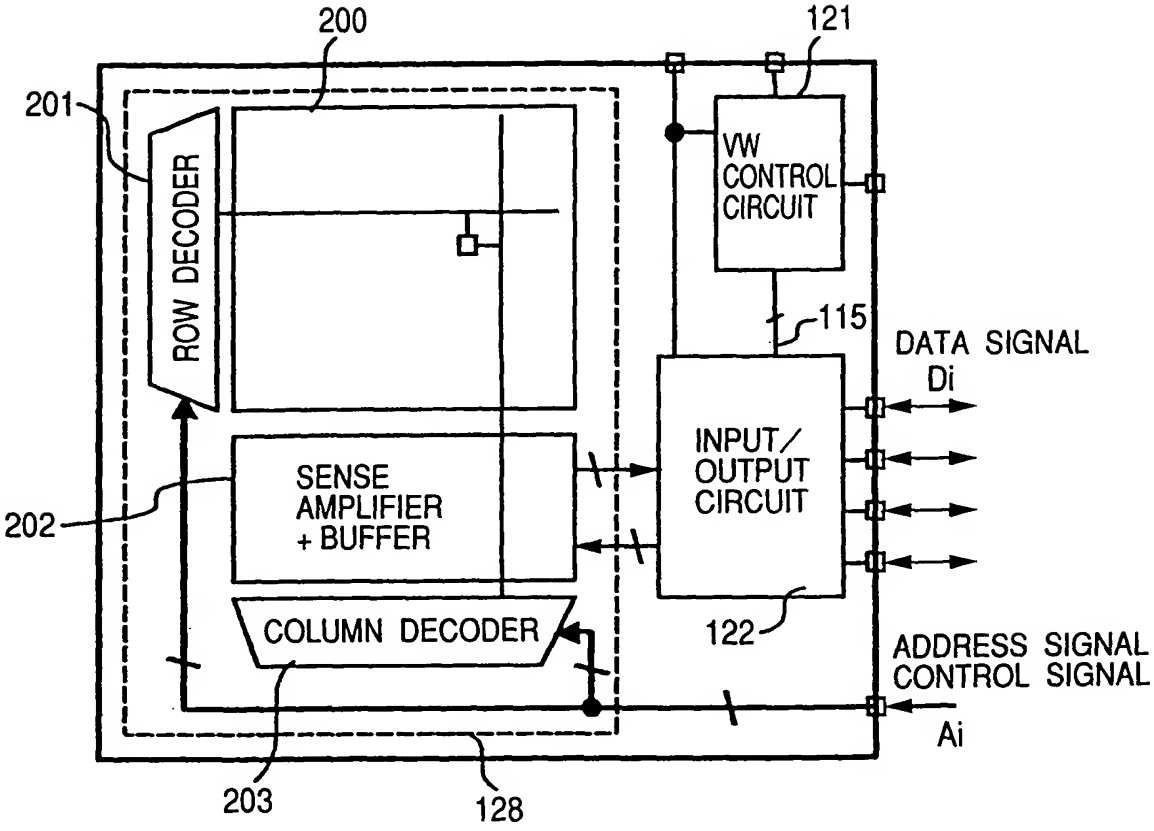
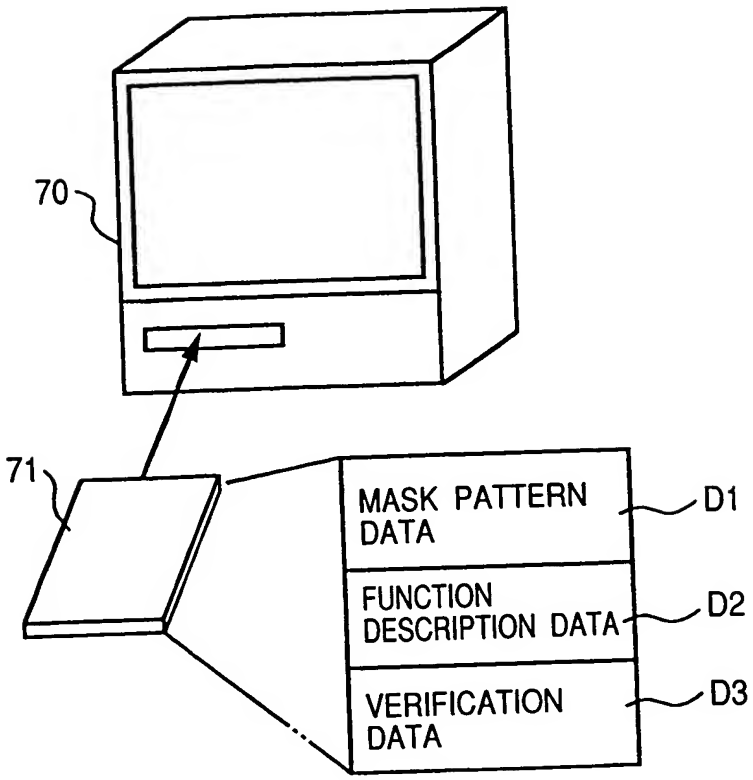

200
121
201
ROW DECODER
VW
CONTROL
CIRCUIT
115
DATA SIGNAL
Di
INPUT/
OUTPUT
CIRCUIT
202
SENSE
AMPLIFIER
+ BUFFER
COLUMN DECODER
122
ADDRESS SIGNAL
CONTROL SIGNAL
Ai
203
128

FIG. 36


70
71
MASK PATTERN DATA
D1
FUNCTION DESCRIPTION DATA
D2
VERIFICATION DATA
D3